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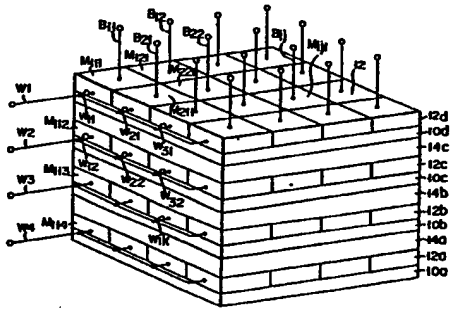
(71) Applicant: TOKYO SHIBAURA DENKI KABUSHIKI KAISHA, 72, Horikawa-cho Saiwai-ku, Kawasaki-shi Kanagawa-ken 210 (JP)

(72) Inventor: Toyama, Masaharu, 3888-10, Akuwa-cho Seya-ku, Yokohama-shi (JP)

(74) Representative: Lehn, Werner, Dipl.-Ing. et al, Hoffmann, Eitle & Partner Patentanwälte Arabellastrasse 4 (Sternhaus), D-8000 München 81 (DE)

(54) Stacked semiconductor memory.

(57) A semiconductor memory is disclosed which has a plurality of memory cells (M) arranged in a stereoscopic matrix shape. The stereoscopic memory cell structure is formed by stacking planar memory cell arrays (12a, 12b, 12c, 12d) each formed of the memory cells aligned in row and column directions. Bit lines (B) extend substantially orthogonally to intersect the layers (10), have the same row and column numbers and commonly connects the linear cell arrays formed of memory cells formed on different layers. Word lines (W) are formed on the same layer and commonly connect the linear cell arrays formed of the memory cells having the same row number. The word lines (W) from the linear cell arrays on the one same layer are combined with one parent word line (W).



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Stacked semiconductor memory

The present invention relates to semiconductor memories and, more particularly, to a stereoscopic semiconductor memory formed by stacking a plurality of semiconductor layers.

A semiconductor memory including a read-only memory (ROM) and a random access memory (RAM) normally has a plurality of memory cells formed on the same plane or surface of a substrate. These memory cells are arrayed in a matrix shape on the surface of the substrate. One linear memory cell array arranged in a row direction of the memory cell matrix are connected commonly to one word line. Similarly, the remaining linear memory cell arrays arranged in the row direction are commonly connected to word lines. On the other hand, the linear memory cell array arranged in a column direction of the memory cell matrix is connected commonly to one bit line. The remaining memory cell arrays arranged in the column direction are similarly connected commonly to the bit lines, respectively. The above-described plurality of word lines and bit lines extend substantially on the same plane or surface on the substrate. More particularly, the word lines and bit lines extend on the plane in parallel relation to the memory cell matrix. The word lines extend in parallel with each other, while bit lines extend in parallel with each other. In other words, the every memory cell is connected to one word

line and one bit line corresponding to the intersection between the word line and the bit line.

When an address signal is inputted to the semiconductor memory, e.g., a dynamic RAM and one word line of the word lines is activated in response to the signal, transfer gates of a plurality of memory cells, contained in the memory cell array connected commonly to the word line, are opened. In this manner, the memory content stored at least one desired memory cell of the memory cells opened at the transfer gates thereof is read by the bit line, or the data supplied to the bit lines can be written or stored in the memory cell opened at the transfer gate thereof.

According to an ordinary semiconductor memory thus composed, since a number of memory cells are arranged substantially on the same plane, the integration determined in response to the area of the surface of the substrate is restricted to a predetermined upper limit. When the memory integration exceeding the upper limit is necessary, it is required to increase the area of the semiconductor substrate, and the profile of a memory cell is undesirably enlarge. In this case, the lengths of the word lines and the bit lines also become lengthened, with the result that a delay of a signal propagation is undesirably take place.

According further to the above-mentioned ordinary semiconductor memory, the number of bit lines to be provided has also a limit. In the above-described dynamic RAM, one bit line may be provided in one memory array extending in the column direction of the memory cell matrix. However, in case of a static RAM, normal and reverse potentials are necessary for one memory array of the column direction as readily understood by those skilled in the art to which the present invention pertains, two bit lines are necessarily provided for each column memory array. Thus, according to the conventional memory configuration, it is difficult to

always obtain sufficient space for such bit lines. This becomes a serious problem in case of sorting the memory content or in case of employing the static RAM as an associative memory. If the allowable number of bit lines capable of forming on the same plane or surface is less than the number of bit lines to be originally necessary, data reading/writing operation should be, in case of large quantity of necessary memory content, sequentially respectively carried out from the end of the memory cell matrix. As a consequence, the time required to read/write the data is increased, and the operating speed of the memory cell is undesirably decreased. Accordingly, the use of such memory cells is limited. For example, this memory cannot be used for the field which indispensably requires high operating speed in the memory such as picture information processing.

It is an object of the present invention to provide a new and improved semiconductor memory which has a large memory capacity and a fast operating speed.

According to a semiconductor memory of the present invention, a plurality of memory cells are arranged in a three-dimensional or stereoscopic matrix shape. The stereoscopic memory cell structure is formed of a plurality of planar memory cell arrays, each having a plurality of memory cells arranged in a matrix shape. These planar memory cell arrays are stacked to be aligned to each other. The first planar memory cell arrays contained in the stereoscopic memory cell structure and substantially parallel to each other are commonly connected to the first wiring pattern. Therefore, the memory cells included in each of the first planar memory cell arrays are connected commonly to one of the first wiring pattern. On the other hand, a plurality of linear memory cell arrays contained in a plurality of second planar memory cell arrays included in the stereoscopic memory cell structure, substantially

perpendicularly crossed with the first planar memory cell arrays and substantially parallel to each other are connected commonly by second wiring patterns. These second wiring patterns extend in the semiconductor memory in the direction substantially perpendicularly crossing with the extending direction of the first wiring patterns. Each of the linear memory cell arrays included in the second planar memory cell arrays is connected commonly to one of the second wiring pattern.

The present invention is best understood by reference to the accompanying drawings, of which:

Fig. 1 is a perspective view showing a part of a dynamic random access memory (RAM) having stereoscopic memory cell structure according to one preferred embodiment of the present invention in a model;

Fig. 2 is a perspective view clearly showing the wires of word lines and bit-lines of the RAM in Fig. 1;

Fig. 3 is a view enlargedly showing one of the linear memory cell arrays having the same row number and column number of the memory cells included in the RAM in Fig. 1 and superposed with each other via semiconductor layers;

Fig. 4 is a perspective view showing a part of the dynamic RAM according to another preferred embodiment of the present invention in a model;

Fig. 5 is a perspective view schematically showing a part of the RAM configuration in Fig. 4 as one example of an address decoder having a laminar structure for the RAM in Fig. 4;

Fig. 6 is a perspective view showing the internal configuration of a part of the address decoder in Fig. 5;

Fig. 7 is a diagram showing an equivalent circuit of the circuit arrangement in Fig. 6; and

Fig. 8 is a view showing one of the linear memory cell arrays having the same row number and column number of the memory cells included in a static RAM according

to a modifaction of the dynamic RAM of Fig. 1, each of the memory cells being included in the linear memory cell formed of flip-flops and the cells being connected commonly to a pair of bit lines.

Referring now to Fig. 1, there is schematically illustrated a dynamic RAM of the laminar semiconductor memory according to one preferred embodiment of the present invention. In Fig. 1, only a part of the semiconductor memory is extracted and shown to readily understand the present invention. Semiconductive layers 10b, 10c, 10d, ... are sequentially stacked and formed on a semiconductor layer or substrate 10a. A plurality of memory cells 12 formed, for example, of MOSFETs are formed in a matrix shape on the surface of each of semiconductor layers 10a, 10b, 10c, 10d, ... The semiconductor layers 10a, 10b, 10c, 10d, ... are electrically insulated from each other by electrically insulative layers 14a, 14b, 14c, ... In other words, a two-dimensional (planar) memory cell array 12 is formed on the semiconductor layer 10a, and a second semiconductor layer 10b is formed on the insulating layer 14a formed on the array 12a. The planar memory cell arrays 12a, 12c, 12d, ... are respectively formed on the semiconductor layers 10b, 10c, 10d, ... similarly to the above and electrically insulated from each other by insulating layers 14.

To suitably show the memory cells arranged in three-dimensional and hence stereoscopical manner, one of memory cells is represented by Mijk (i = 1, 2, 3, ..., j = 1, 2, 3, ..., k = 1, 2, 3, ...). The letter "i" designates the row number of the planar cell array formed on one of semiconductor layer. The letter "j" denotes the column number of the planar cell arrays. The letter "k" designates the number of the planar cell arrays superposed in laminar state, and in Fig. 1, the planar cell array disposed on the uppermost layer is denoted by k = 1.

In Fig. 1, the memory cells included in the planar memory cell array 12d formed on the semiconductive layer 10d drawn to be disposed at the uppermost stage are connected to a word line W1. The memory cells M111, M121, ... forming the first row of a plurality of memory cells included in the planar cell array 12d and arranged in matrix shape are connected commonly to the word line w11. The word line w11 is formed in accordance with the prior art to extend substantially in parallel with the surface of the layer 10d. The linear cell array, formed of memory cells M211, M221, ... forming the second row of the memory cells included in the planar cell array 12d, is connected commonly to the word line w21. Similarly to the above, all the linear row cell arrays included in the planar matrix array 12d are respectively connected commonly to the word lines w31, ... The word lines w11, w21, w31, ... are combined with the single word line (parent word line) W1 at the position in the vicinity of the planar cell array 12d substantially out of the planar cell array 12d. In other words, one word line W1 is branched to a plurality of word lines w11, w21, w31, ... at the above-described predetermiend position, and the branched word lines w11, w21, w31, ... are electricaly commonly connected between the memory cells linearly arranged in the row direction of a plurality of memory cells included in the planar cell array 12d. The word line W1 and a plurality of word lines w11, w21, w31, ... branched from the parent word line W1 are included in an imaginary plane substantially parallel to the surface of the semiconductive layer 10d.

A plurality of word lines w12, w22, w32, ... are each connected in the similar manner to the above to a plurality of linear row cell arrays of planar cell array 12c formed on the semiconductive layer 10c formed to be electrically isolated by the insulating layer 14b from the layer 10c under the semiconductive layer 10d. These word lines w12, w22, w32, ... are combined with one

parent word line W2. Similarly to the above, the word lines W3, W4 are connected to the other planar cell arrays 12b, 12a. The connecting state of the word lines are understood more clearly with reference to the model view of the semiconductor memory exploded and designated virtually in the respective memory cells in Fig. 2.

In Fig. 1, a plurality of bit lines B are further connected to the above-described memory cell structure connected with the above word lines W1, W2, W3, W4. These bit lines B substantially extend perpendicularly to the branched word line patterns. In other words, each of bit lines Bij (i = 1, 2, 3, ..., j = 1, 2, 3, ...) is perpendicularly extended to the planar cell arrays 12 each formed on the semiconductor layers 10, and connected commonly to the stacked memory cell group arranged to be linearly aligned to each other in a direction substantially perpendicularly to one of the planar memory cell arrays 12. The bit line B11 of the bit lines Bij, for example, connects commonly one memory cell M111, included in the planar cell array 12d, a memory cell M112 included in the planar cell array 12c and disposed directly under the memory cell M111, a memory cell M113 included in the planar cell array 12b and disposed directly under the memory cell M112, and a memory cell M114 included in the planar cell array 12a and disposed directly under the memory cell M113 through the semiconductor layers 10d, 10c, 10b. The connecting state of the memory cell structure of the bit line B11 is further clarified with reference to Fig. 2. The other bit lines including the bit lines B12 and bit lines B21, ... are provided substantially perpendicularly crossed to the word line patterns or the planar cell array 12 in the similar manner to the above.

In other words, the memory cells Mij1, Mij2, Mij3, Mij4 formed respectively on the same semiconductor layers 12 of the memory cells of the semiconductor

memory in Fig. 1 are eventually respectively connected commonly to the parent word lines W1, W2, W3, W4. On the other hand, the memory cells M11k, M12k, ..., and M21k, M22k, ... having the same row number and column number and formed on the different semiconductor layer are respectively connected commonly to the bit lines B11, B12, ..., B21, B22, ... Accordingly, when an address signal is supplied, one word line of the above word lines Wk is activated in response to the signal. Therefore, when one word line, e.g., word line W1, is activated, all the memory cells Mij1 included in the planar cell array 12d connected to the word line W1 is activated and the transfer gates thereof are caused to open. In this state, at least one bit line Bij = B12 is designated for one desired memory cell, e.g., M121 of these memory cells Mij1, the digital data supplied to the bit line B12 can be written. The digital data stored as described above in the memory cell M121 can be read out by designating the bit line B12 at desired time similarly.

According to the dynamic RAM as one preferred embodiment of the present invention thus constructed, the memory cells Mijk are arranged in three-dimensionally or stereoscopically, and one planar cell array formed on the same semiconductor layer is connected commonly to the same word line Wk. The bit lines Bij extend substantially perpendicularly to the word line pattern and connect commonly the memory cells Mij1, Mij2, ..., Mijk, ... having the same row number and column number and formed on the different layers. Accordingly, the memory capacity can be increased as compared with the conventional memory element formed of the memory cells formed in two-dimensional manner on one semiconductive layer. Further, since the region capable of connecting the bit line for the stacked cell structure extends planarly, a number of bit lines may be readily connected to the stacked cell structure. This

is convenient for the data sorting or image information processing.

In other words, in the stacked memory cell structure shown in Figs. 1 and 2 and described in detail above, the word lines branched from one parent word line determines one virtual plane, to be named word-line routing plane, in which all the word lines branched from one parent word line are involved. The word lines w11, w21, w31, ... which are branched from the parent word line W1 determines one word-line routing plane, say P1, in which the word lines w11, w21, w31, ... are involved. The word lines w12, w22, w32, ... which are branched from the parent word line W2 determines one word-line routing plane, say P2, in which the word lines w12, w22, w32, ... are involved. More generally, the word lines w1k, w2k, w3k, ... which are branched from the parent word line Wk determines one word-line routing plane Pk in which the word lines w1k, w2k, w3k, ... are involved. All these word-line routing planes P1, P2, ... which are assigned to parent word lines W1, W2, ..., respectively, are stacked and superposed substantially parallel to one another so that the word lines wi1, wi2, wi3, ... which belong to the same row number "i" but to different word-line routing planes P1, P2, P3, ..., respectively, are superposed to one after another. In other words, the word lines wi1, wi2, wi3, ... determine one second word-line routing plane Qi in which all the word lines belonging to the same row number "i" are involved, and all the second word-line routing planes Qi's are substantially orthogonal to the first word-line routing planes Pk's. Bit lines Bij are situated substantially perpendicularly to all the first word-line routing planes Pk's. In the conventional memory cell array structure formed in two-dimensional manner on one semiconductor layer, both word lines and bit lines are arranged in two-dimensional manner, that is to say, word lines are substantially arranged in one plane while bit

lines are substantially arranged in another plane, and both planes are superposed parallel to each other or substantially form one common plane. In the stacked memory cell structure shown in Figs. 1 and 2, word lines and bit lines are arranged mutually in three-dimensional manner as described above in detail, and this three-dimensional routing scheme makes it possible to connect a much larger number of bit lines for an ensemble of memory cells than the conventional two-dimensional routing scheme does.

Further, a plurality of word lines wik drawn from each of the planar cell arrays are combined respectively with the parent word lines Wk corresponding to the number of the planar cell arrays. In other words, the memory cells included in the each planar cell array are respectively branched and connected commonly to one of the parent word lines Wk. In this manner, total word line length can be shortened, and hence the delay of the signal propagation speed can be reduced even at the terminal. Further, since the bit lines Bij are not necessarily laid complicatedly among the cells, the line length can be shortened. Therefore, the operating speed of the memory element can be improved.

Fig. 3 illustrates one of the cell groups of a series of memory cells having the same row number and column number and formed in different planar cell array 12 in the memory cell structure of Fig. 2 particularly extracted. For the purpose of illustration only, memory cells M111, M112, M113, M114 are selected, and word lines w11, w12, w13, w14 are respectively connected to these memory cells. In Fig. 3, each of the memory cells M111, M112, M113, M114 includes one MOSFET and one capacitor.

Fig. 4 illustrates a dynamic RAM according to another preferred embodiment of the present invention, wherein the like reference numerals designate the same or equivalent parts and components in Figs. 1 and 2, and

will be omitted in description.

The same bit line Bjk (e.g., bit line B11) is connected commonly to a series of memory cells (e.g., memory cells M111, M211, M311, M411) having the same column number formed on the same semiconductor layer (e.g., layer 10d) in a plurality of memory cells Mijk included in the RAM in Fig. 4. Accordingly, a series of cells M111, M211, M311, M411, for example, are connected commonly to one bit line B11, a series of memory cells M121, M221, ... are connected to one bit line B21, a series of memory cells M131, M231, ... are connected to a bit line B31, and a series of memory cells M141, ..., M441 are connected commonly to the bit line B41 in the planar cell array 12d formed on the semiconductor layer 10d. These series of bit lines B11, B21, B31, B41 extend substantially parallel to each other, and are formed substantially parallel to the planar cell array 12d formed on the semiconductor layer 10d. In other words, the memory cell Mij1 included in the planar cell array 12d is divided into a plurality of linear column cell arrays having the same column number and respectively connected commonly to the bit lines Bj1.

The bit lines B12, B22, ..., bit lines B13, B23, ... and bit lines B14, ..., B44 are connected commonly to a plurality of linear column cell arrays having the same column number in the same manner as above in the planar cell arrays 12c, 12b, 12a, respectively.

On the other hand, a series of memory cells having the same row number of the memory cells included in each of planar cell arrays 12 are connected commonly to the same word lines wik. Further, a plurality of word lines w1k, w2k, w3k, w4k for respectively connecting a series of memory cell groups, each of which consists of linear cell arrays superposed to be elevationally aligned through the semiconductor layers 10, and insulating layers 14 are combined with one parent word line W1, W2, W3, W4. For example, in Fig. 4, a word line w11 for

commonly connecting the linear row cell array of a series of memory cells M111, M121, M131, M141 having the same row number of the planar cell array 12d on the semiconductor layer 10d, a word line w12 for commonly connecting the memory cells M112, M122, M132, M142 linearly extending in parallel with the linear row cell array under the memory cells M111, M121, M131, M141 arranged linearly in series included in the planar cell array 12c, and word lines w13 and w14 for commonly connecting the memory cells M113, ... and M114, ... superposed with the memory cells M111, M121, M131, M141 forming the linear cell arrays included in the planar cell arrays 12b, 12a are combined with one parent word line W1. In other words, the line pattern formed of the word lines w11, w12, w13, w14 branched from the parent word line W1 substantially intersect the planar cell arrays 12 or the above bit lines B formed respectively on the semiconductor layers 10.

Other series of word lines w21, ..., w24 are similarly combined with one parent word line W2. Further, other series of word lines w31, ..., w34 and the other series of word lines w41, ..., w44 are respectively combined with the parent word lines W3 and W4.

In this manner, even in the stereoscopic memory cell structure connected to the bit lines Bjk and word lines Wi, the writing/reading of the digital data can be carried out similarly to the above-described embodiments.

According to the dynamic RAM in Fig. 4, the word line patterns branched from each of parent word lines Wi substantially intersect the planar cell array or bit lines B formed respectively on the semiconductor layers 10. Therefore, to drive the RAM thus constructed, an address decoder 20 designated, for example, in Fig. 5 is employed.

According to the address decoder in Fig. 5, decoder elements 22 are provided correspondingly to the planar

cell arrays 12a, 12b, 12c, 12d superposed in laminar or stacked state with each other as described above. Reference numerals A1, A2 denote address input lines, and reference numerals $\overline{A1}$, $\overline{A2}$ designate inverting signal lines. The line pattern formed of these lines A1, $\overline{A1}$, A2, $\overline{A2}$ extend in parallel with each other and are included in a plane substantially vertical to the planar cell arrays 12 formed respectively on the semiconductor layers 10.

Fig. 6 illustrates a circuit block section 23 particularly extracted correspondingly to the word lines w31, w32, w33, w34 in the above RAM (Fig. 4) of the address decoder 20 in Fig. 5. The parent word line W3 combined with the word lines w31, ..., w34 is activated when the digital levels of the address lines A1, A2 respectively become "0" and "1". The stereoscopic circuit in Fig. 6 includes n-channel type FETs 24, 26 and p-channel type FETs 24', 26' to form 2-input C-MOS NOR circuit. "high" power voltage V_{DD} is supplied to the first power line 28 connected to the p-channel type FET 24'. "low" power voltage V_{SS} is applied to the second power line 30 connected to the n-channel type FETs 24, 26. In Fig. 6, electrically conductive connect lines L for electrically connecting between the FETs are shaded only for the purpose of readily distincting visually from the other section. In other words, n-channel type FETs 24 and 26 are connected in parallel with each other via the connect lines L1 and L2. The p-channel type FETs 24' and 26' are connected in series with each other via connect line L3. The connect line L4 connects between the n-channel type FET 26 and the p-channel type FET 26'. Accordingly, the FETs 24 and 24' are driven by the signal supplied from the input line A1, and the other FETs 26 and 26' are driven by the signal supplied from the inverting signal line $\overline{A2}$. No FET is provided in the circuit structure 23 in Fig. 6 corresponding to the remaining inverting signal line $\overline{A1}$ and

input line A2. An equivalent circuit of the section of the address decoder in Fig. 6 thus constructed is shown in Fig. 7.

According to the circuit structure 23 of a part of the address decoder thus constructed, the word lines w31, ..., w34 are activated when the address input (A1, A2) becomes (0, 1). In this state, the word lines w31, ..., w34 are connected directly to one connect line L2 for connecting between the FETs 24 and 26 included in the decoder of Fig. 6 in their drain regions. In other words, the connect line L2 included in the address decoder substantially serve as the above-described parent word line W3. Accordingly, it is not necessary to newly provide a parent word line W3. It is not necessary by the same reason to newly provide other parent word lines W1, W2, W4. Therefore, the connection between the RAM in Fig. 4 and the address decoder in Fig. 5 can be efficiently performed, and the total line length can be shortened, thereby improving the signal propagation speed.

Although the parent invention has been shown and described with respect to particular embodiments, nevertheless, various changes and modifications which are obvious to a person skilled in the art to which the invention pertains are deemed to line within the spirit, scope, and contemplation of the invention. In the embodiments described above, the dynamic RAM is shown and described. However, the present invention is not limited to the particular RAM, but may also be applied for other memory elements such as, for example, a static memory, a read-only memory, etc.

Fig. 8 illustrates one of the cell groups of a series of memory cells having the same row number and column number and formed in different planar cell array in the static type memory cell structure according to a modification of the preferred embodiment of the invention of Fig. 1 particularly extracted. For the purpose

of illustration only, memory cells M'_{111}, M'_{112}, M'_{113}, M'_{114} are selected, and word lines w11, w12, w13, w14 are respectively connected to these memory cells. In Fig. 8, each of the memory cells M'_{111}, M'_{112}, M'_{113}, M'_{114} is applied with a flip-flop formed of MOSFETs, and a pair of bit lines B11 and $\overline{B11}$ are used as these memory cells. Voltage signals different from each other are supplied to these bit lines B11 and $\overline{B11}$.

Claims:

1. A semiconductor memory having a plurality of memory cells (M) for electrically storing data, characterized in that said plurality of memory cells (M) are arranged in a three-dimensional matrix, the three-dimensional memory cell structure is formed of a plurality of planar memory cell arrays (12) aligned and stacked with a plurality of memory cells (M) arranged in a matrix shape in a direction substantially perpendicularly to the planar memory cell arrays; and that said semiconductor memory comprises a plurality of first wiring means (w) for commonly connecting each of a plurality of first planar memory cell arrays substantially parallel with each other, memory cells (M) included in each of the first planar memory cell arrays being connecting commonly to one of said first wiring means (w), and a plurality of second wiring means (B) for respectively commonly connecting a plurality of linear memory cell arrays which are included in a plurality of second planar memory cell arrays substantially orthogonally intersecting the first planar memory cell arrays and which substantially orthogonally intersect the first planar memory cell arrays, said linear memory cell arrays extending substantially parallel to each other and each of the linear memory cell arrays included in the second planar memory cell arrays being connected commonly to one of said second wiring means (B).

2. A semiconductor memory according to claim 1, characterized in that each of said first wiring means comprises a plurality of third wiring means (w) for respectively commonly connecting memory cell groups included in a plurality of second linear memory cell arrays arranged substantially in a direction perpendicularly extending to said second planar memory cell arrays in the memory cells included in each of said first planar memory cell arrays (12), said third wiring

means (w) being electrically conducted with each other.

3. A semiconductor memory according to claim 2, characterized in that said plurality of third wiring means (w) extend in parallel with each other and substantially in parallel with said first planar memory cell arrays.

4. A semiconductor memory according to claim 3, characterized in that said first wiring means further comprises fourth wiring means (W) for electrically connecting said third wiring means (w) each connected to the second linear memory cell arrays included in said each of the first planar memory cell arrays (12) at the position corresponding to substantially externally of said memory cell structure.

5. A semiconductor memory according to claim 4, characterized in that said fourth wiring means (W) are provided corresponding to said plurality of the first planar memory cell arrays.

6. A semiconductor memory according to claim 4, characterized in that said first planar memory cell arrays are each formed on a plurality of layers (10) electrically isolated from each other, said layers are sequentially stacked to have a laminar structure.

7. A semiconductor memory according to claim 4, characterized in that said first planar memory cell arrays are formed to substantially orthogonally intersect a plurality of layers (10) electrically isolated from each other, said layers are sequentially stacked to form a laminar structure.

8. A semiconductor memory according to claim 6, characterized in that said plurality of second wiring means (B) extends to substantially orthogonally intersect said layers (10) for commonly connecting said plurality of first linear memory cell arrays included in said second planar memory cell arrays.

9. A semiconductor memory system comprising a semiconductor memory and decoder means (20) for

receiving an address input signal and for activating desired memory cells of said semiconductor memory, characterized in that said semiconductor memory comprises a plurality of layers (10) electrically isolated from each other and sequentially stacked to form a laminar structure, a plurality of cell matrix structures (12) having a plurality of memory cells aligned in row and column directions on the surfaces of said layers, a plurality of bit lines (B) for commonly connecting a plurality of the first linear memory cell arrays respectively formed of memory cells arranged in the same column direction of the memory cells included in the cell matrix structure on each of said layers, and a plurality of word lines for commonly connecting a plurality of second linear memory cell arrays formed of memory cells arranged in the same row direction of the memory cells included in the memory cell matrix structure on each of said layers and substantially orthogonally intersecting the first linear memory cell arrays, and that said decoder means (20) is electrically connected through said word lines (w) to said semiconductor memory, stacked correspondingly to laminar units formed respectively of said plurality of second linear memory cell arrays stacked via said layers and formed by arranging in parallel with each other a plurality of linear decoder element arrays respectively formed of a plurality of stacked decoder elements (22) including active elements (24, 24', 26, 26'), each of said linear decoder element arrays including wiring means (L2) for commonly connecting said plurality of word lines (w31, w32, w33, 34) which respectively connect a plurality of second linear memory cell arrays stacked with each other and included in each of said laminar units corresponding to the linear decoder element array and for connecting between predetermined said active elements (24, 26) provided therein, said wiring means (L2) extending to substantially orthogonally intersect said layers (12).

FIG. 1

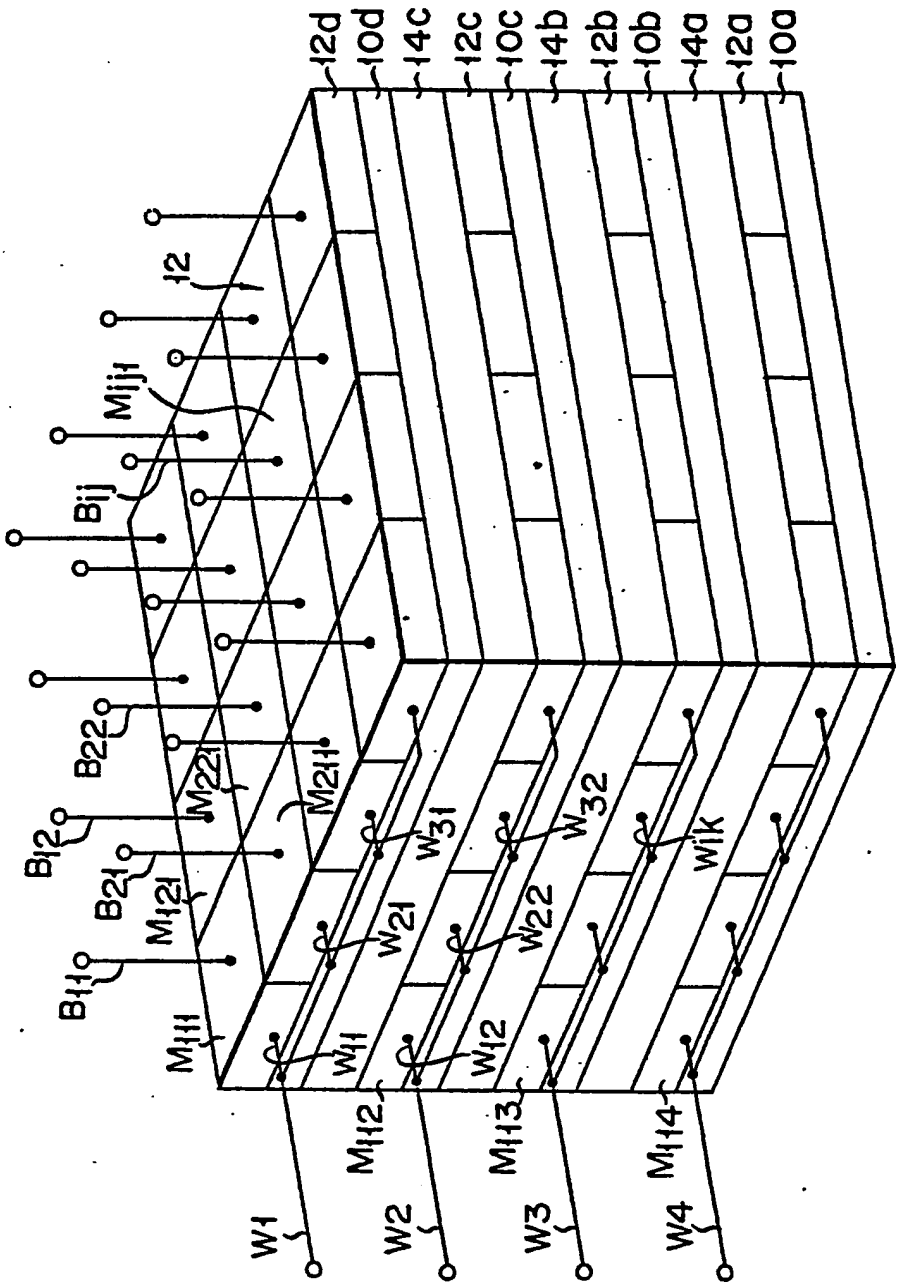
12d
10d
14c
12c
10c
14b
12b
10b
14a
12a
10a
12
Mijj
Bij
B22
M221
M211
B12
B21
M121
B110
M111
W11
W21
W31
W12
W22
W32
Wik
M112
M113
M114
W1
W2
W3
W4

FIG. 2

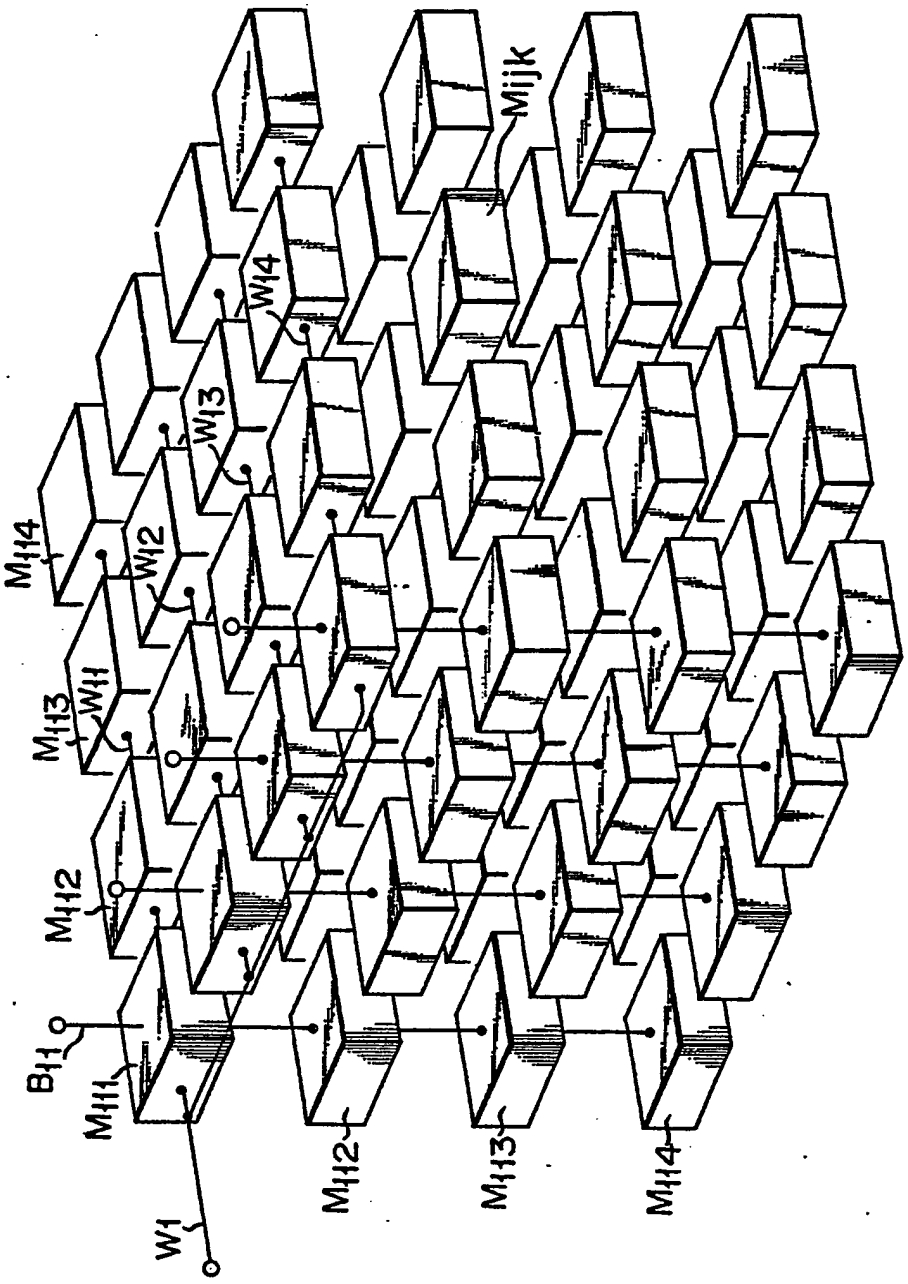

FIG. 3

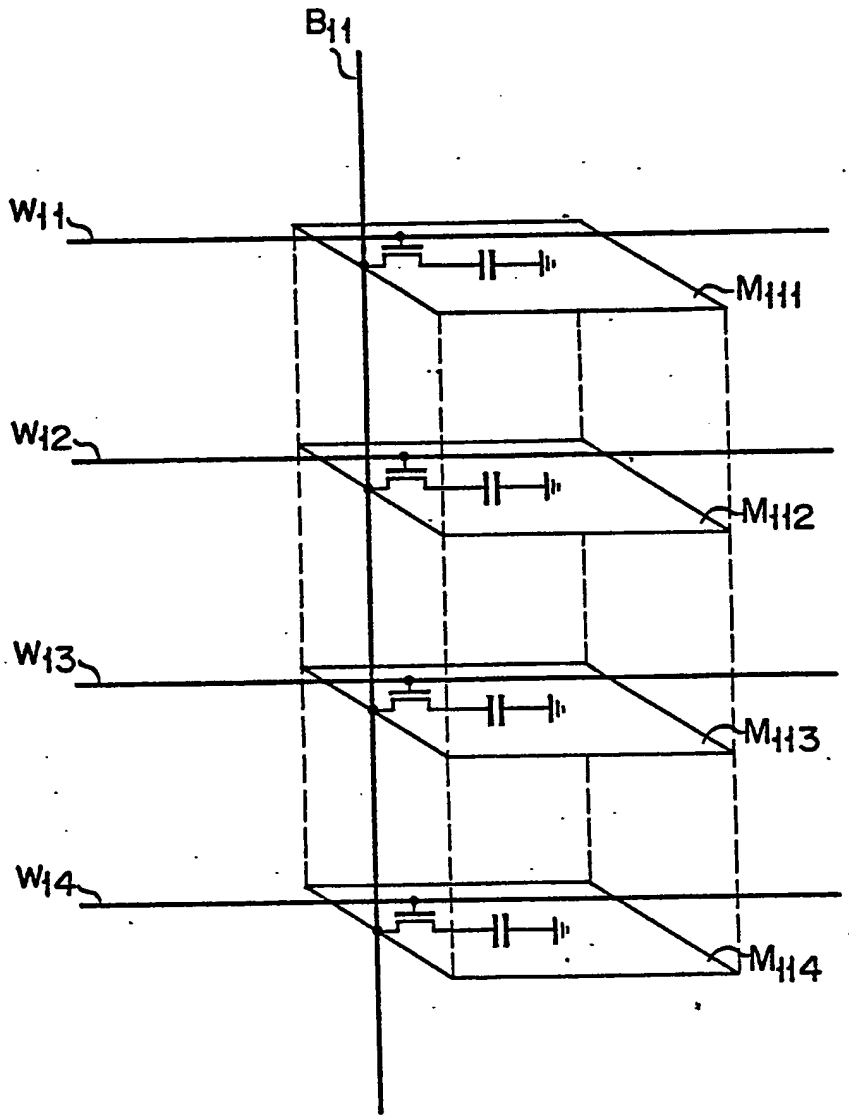

FIG. 4

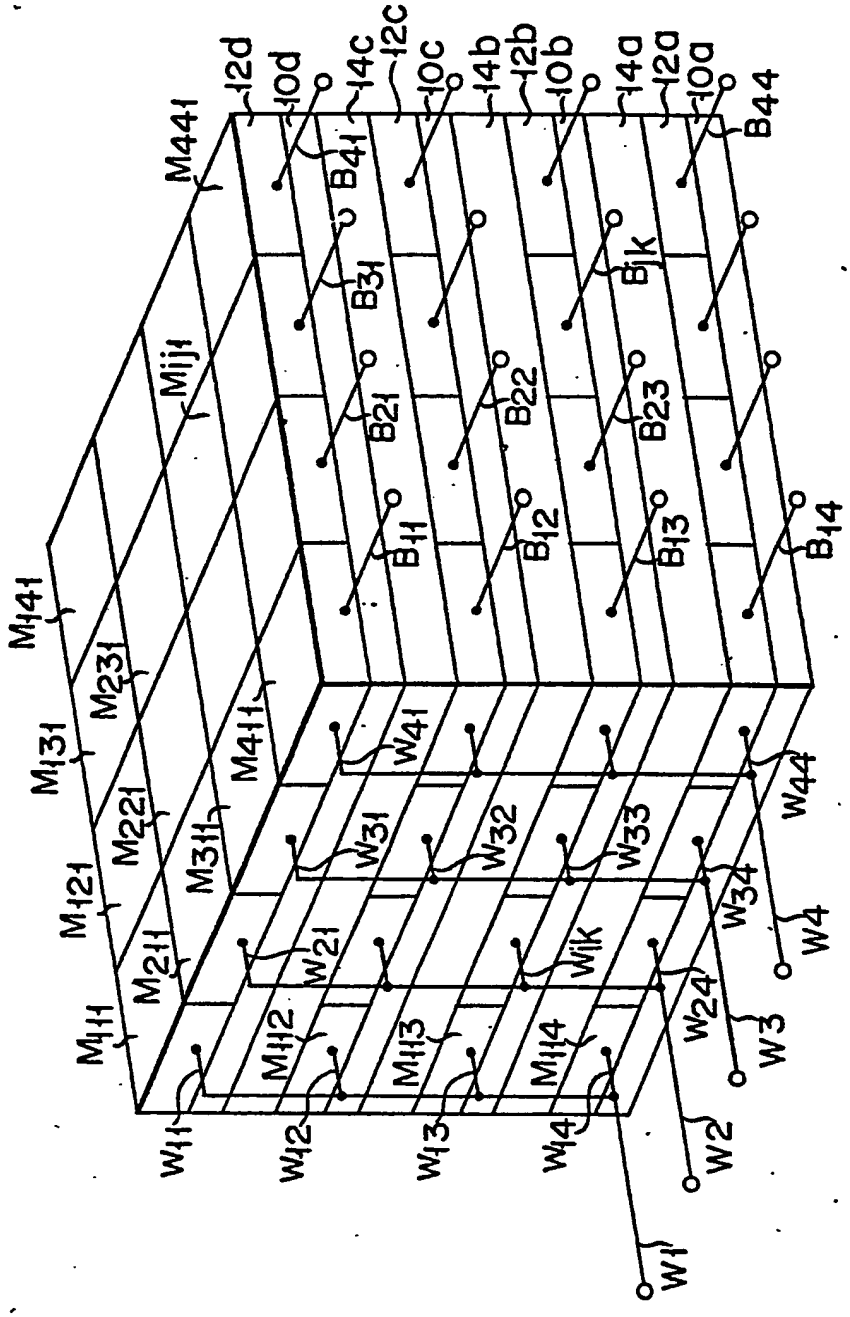
12d
10d
14c
12c
10c
14b
12b
10b
14a
12a
10a
M441
B41
B44
B31
Bjk
Mijj
B21
B22
B23
M141
M231
B11
B12
B13
B14
M131
M411
W41
M221
M311
W31
W32
W33
W44
M121
W34
W4
M211
W21
Wik
W24
M111
M112
M113
M114
W3
W11
W12
W13
W14
W2
W1

FIG. 5

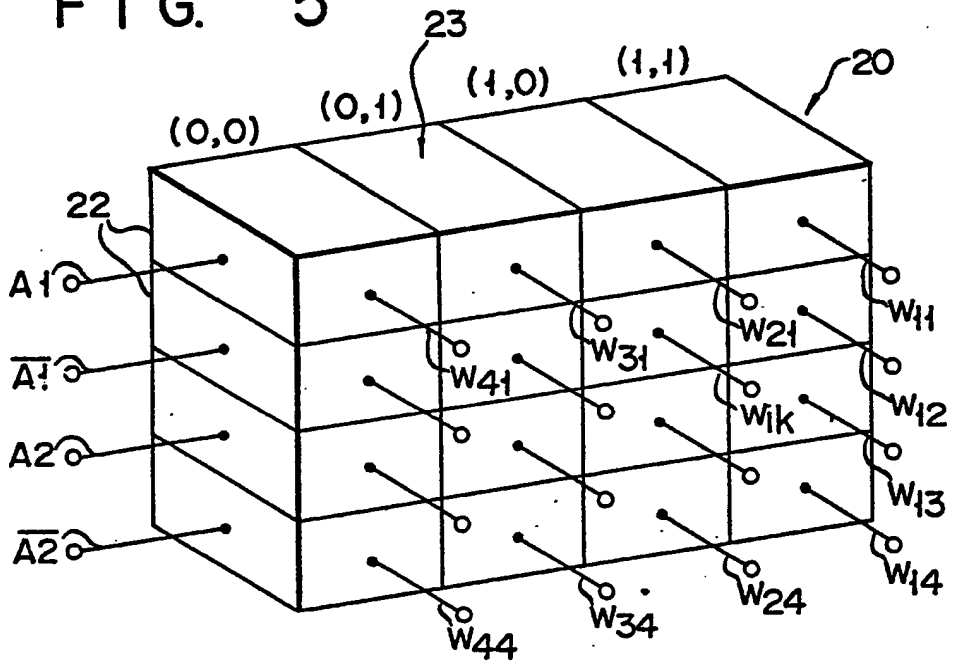
23
(0,0)
(0,1)
(1,0)
(1,1)
20
22
A1
$\overline{A1}$
A2
$\overline{A2}$
W_{11}
W_{12}
W_{13}
W_{14}
W_{21}
W_{31}
W_{41}
W_{1K}
W_{24}
W_{34}
W_{44}

FIG. 6

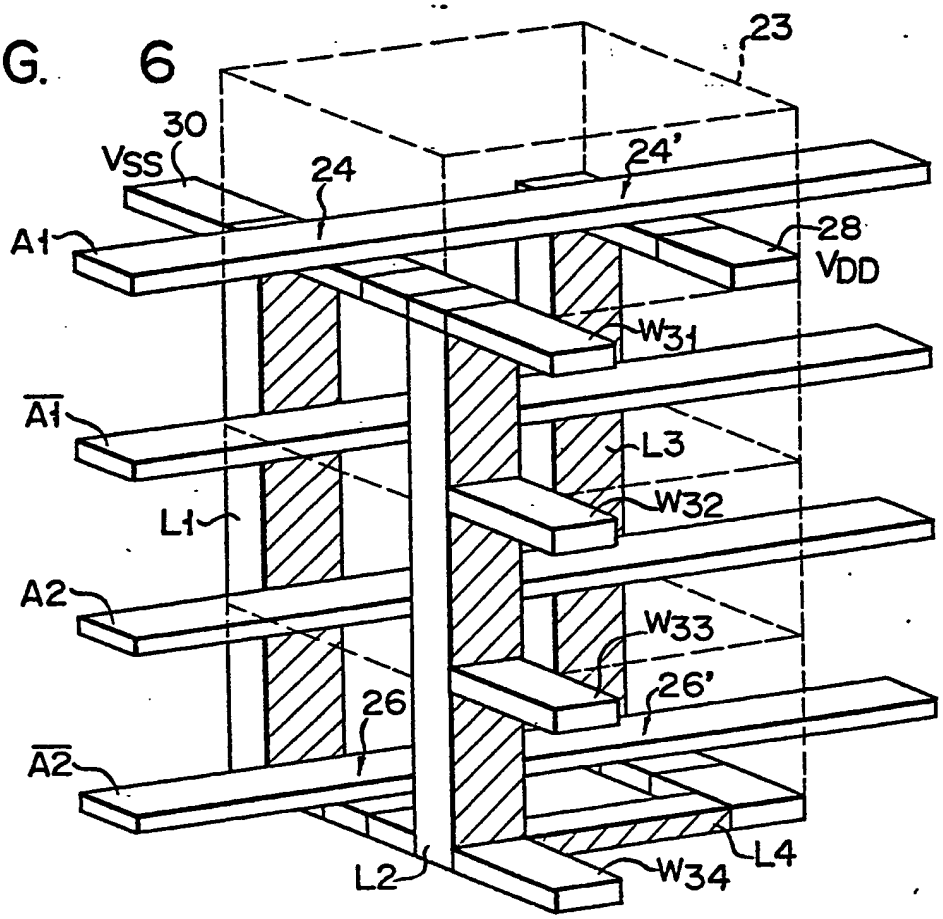
23
30
VSS
24
24'
A1
28
VDD
W_{31}
$\overline{A1}$
L3
W32
L1
A2
W33
26'
26
$\overline{A2}$
L4
L2
W34

FIG. 7

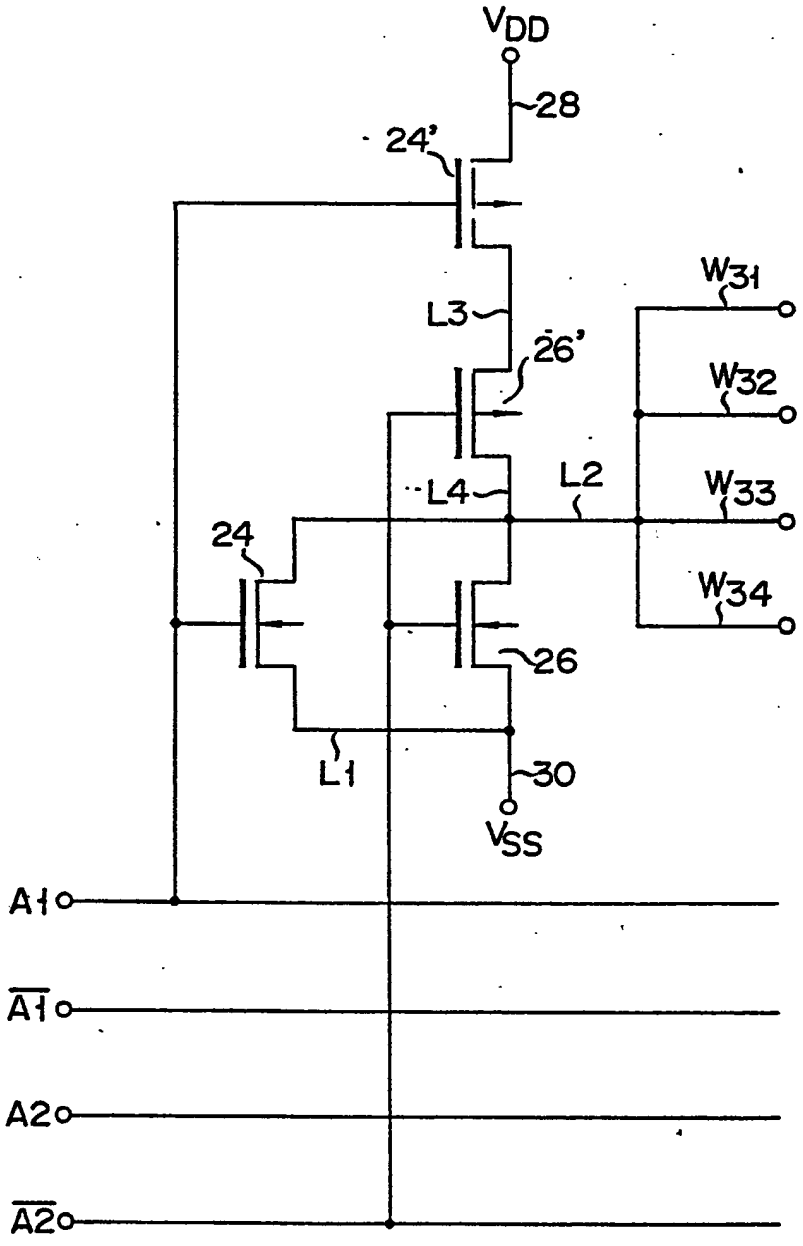
VDD
28
24'
W31
L3
26'
W32
L4
L2
W33
24
W34
26
L1
30
VSS
A1
$\overline{A1}$
A2
$\overline{A2}$

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FIG. 8